SPECIFICATION AMENDMENTS

Please replace the paragraph beginning on page 14, line 24 and ending on page 15, line 5, with the following amended paragraph:

The exemplary embodiment of the buffer device according to the invention which is shown in Fig. 2 has n-1 identical latch stages ~~L1~~ L2 to Ln-1 which all have the structure of the latch stage L1 shown in Fig. 1 and are illustrated only schematically here. The signals D_{in}, READ, CLK and/or LAT are fed via lines 4, 4a, 4b and 4c and via corresponding taps 25a, 25b, 25c, 26 and 27 to the respective latch devices 6 and to the multiplexers 7 integrated therein.

Please replace the paragraph on page 15, lines 7-12, with the following amended paragraph:

The multiplexers 7 of the latch stages ~~L1~~ L2 to Ln-1 of the embodiment in Fig. 2 according to the invention are each integrated into regions 20 of feedback loops provided for buffering in the latch devices 6. These regions 20 of the feedback loops are illustrated only schematically in the embodiment in Fig. 2.